REMARKS

The paragraphs on pages 8, 10, and 11 are amended due to typographic errors. Figs. 2 and 3 are amended according to the amended specification. A proposed drawing change is attached. No new matter is entered. Approval is requested.

Claims 1 and 7 are currently amended by incorporating limitations of the control signals. Support for the amendment is shown in page 7, line 5 to page 8, line 6 and Fig. 3.

Claim 11 is newly added. Support for the newly added claim 12 may be found in page 7, line 5 to page 8, line 6 and Fig. 3.

Claims 1, 3-7, and 9-10 stand rejected under 35 U.S.C. 102(e). Claims 2 and 8 stand rejected under 35 U.S.C. 103(a). These rejections are discussed below.

Claim Rejections

Claim 1 stands rejected under 35 U.S.C. 102(e) as being anticipated by ***Nakajima*** et al. (U.S. Patent No. 6,664,943). The Applicant respectfully traverses the 35 U.S.C. 102(e) rejections for at least the following reasons.

Nakajima **does not teach, disclose or suggest a comparator corresponding to the n-th control signals among a plurality of control signals and receiving the (n-1)-th control signals among the plurality of control signals.**

According to Figs. 1 and 18 of ***Nakajima***, a comparator 100 receives input signals in1 and in2 to compare the voltage at modes 1 and 2. The comparator 100 only receives the corresponding sampling pulse SP, and it is not controlled by a corresponding control signal and does not receive a pre-stage control signal to reset the comparator 100.

According to amended claim 1, a pulse generator generates a sample pulse which samples in time series an input digital signal corresponding to a pixel and generates a plurality of control signals. A comparator is controlled by the n-th control signals from among the plurality of control signals and receives the (n-1)-th control signals and a corresponding sampling pulse. (Support for the limitation is in the amended specification and the amended Fig. 3.) A comparator 204-2 of the second stage (n-th) receives a corresponding sampling pulse. Moreover, the comparator 204-2 of the second stage (n-th) is controlled by a signal SR_out2 and receives a signal SR_out1 which is used to control a comparator 204-1 of the first stage. The comparator 204-2 not only receives the corresponding sampling pulse and the signal SR_out2, but also the signal SR_out1 of the pre-stage.

It is respectfully submitted that for this reason, *inter alia*, claim 1 patently defines over the applied art, and the rejection of claim 1 should be withdrawn.

Claim 7 stands rejected under 35 U.S.C. 102(e) as being anticipated by ***Nakajima*** et al. (U.S. Patent No. 6,664,943). The Applicant respectfully traverses the 35 U.S.C. 102(e) rejections for at least the following reasons.

Nakajima **does not teach, disclose or suggest the n-th comparator among a set of comparators which is controlled by the n-th control signals among a plurality of control signals and receives the (n-1)-th control signals among the plurality of control signals.**

According to Figs. 1 and 18 of ***Nakajima***, a comparator 100 receives input signals in1 and in2 to compare the voltage at modes 1 and 2. The comparator 100 only receives the corresponding sampling pulse SP, and it is not controlled by a corresponding control signal and does not receive a pre-stage control signal.

According to amended claim 7, a shift register generates a sample pulse which samples in time series an input digital signal corresponding to a pixel and generating a plurality of control signals. Each of a set of comparators is controlled by the n-th control signals from among a plurality of control signals and receives the (n-1)-th control signals among the plurality of control signals and a corresponding sample pulse. Support for the limitation is shown in the amended specification and the amended Fig. 3. For example, a comparator 204-2 of the second stage (n-th) receives a corresponding sample pulse. Moreover, the comparator 204-2 of the second stage (n-th) is controlled by a signal SR_out2 and receives a signal SR_out1 which is used to control a comparator 204-1 of the first stage. The comparator 204-2 not only receives the corresponding sampling pulse and the corresponding sampling pulse, but also a pre-stage control signal SR_out1.

It is respectfully submitted that for this reason, *inter alia*, claim 7 defines over the applied art, and the rejection of claim 7 should be withdrawn.

According to the specification and the Fig. 3, a shift register 222 generates a sample pulse which samples in time series an input digital signal corresponding to a pixel and generating a plurality of control signals SR_out1 to ST_out3. A comparator 204-2 of the second stage (n-th) is controlled by a signal SR_out2 and receives a signal SR_out1 which is used to control a comparator 204-1 of the first stage. The operation of the signal SR_out1 for the comparator 204-2 is resetting the comparator 204-2. Accordingly, claim 11 is newly added to include the limitation of that the n-th comparator from among a set of comparators is controlled by the n-th control signal of a plurality of control signals and is reset by the (n-1)-th control signals among the plurality of control signals. The features of new claim 11 are not disclosed by the applied art.

Conclusion

For the reasons as described above, the Applicant believes that claim 1 is allowable over the cited reference. Insofar as claim 1 is allowable, claims 2-6, all depend from claim 1 and its related claims, including every claimed element thereof, are also allowable on their own merits in claiming additional elements not included in claim 1. Moreover, for the reasons as described above, the Applicant believes that claim 7 is allowable over the cited reference. Insofar as claim 7 is allowable, claims 8-10, all depend from claim 7, including every claimed element thereof, is also allowable on its own merits in claiming additional elements not included in claim 4. Moreover, for the reasons as described above, the Applicant believes that newly added claim 11 is allowable.

Withdrawal of the rejections and allowance of the claims, as now amended, are respectfully requested. Applicant has made every effort to place the present application in condition for allowance. It is therefore earnestly requested that the present application, as a whole, receive favorable consideration and that all of the claims be allowed in their present form.

Respectfully submitted,

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